THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KARL M. GUTTAG
and CHRISTOPHER J. READ

Appeal No. 1996-3193
Application 08/160,112[1]

ON BRIEF

Before JERRY SMITH, BARRETT, and FLEMING, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

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[1] Application for patent filed November 30, 1993, entitled "Method, Apparatus And System For Sum Of Plural Absolute Differences."

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1 and 3-12. Claims 2 and 13-34 have been canceled.

We affirm-in-part.

BACKGROUND

The disclosed invention is directed to a method for forming the sum of the absolute value of the difference between a pair of numbers in respective first and second sets of numbers. The invention is described in the specification at page 268, line 29, through page 281, line 3, with respect to figure 47.[2]

Claim 1 is reproduced below.

> 1. A method for forming a sum of the absolute value of the difference between each pair of numbers of respective first and second sets of numbers, said method comprising the steps of:
>
> forming the difference between a first number of the first set of numbers of said number pair and a second number of the second set of numbers of said number pair;
>
> setting a status bit to a first digital state if said difference is greater than zero;
>
> resetting said status bit to a second digital state if said difference is less than zero;

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[2] Appellants may wish to change "loop up" to "look up" at page 272, line 18, of the specification.

conditionally either 1) adding said difference to a running sum of the absolute values of the differences if said status bit is said first digital state, or 2) subtracting said difference from the running sum of absolute values of the differences if said status bit is said second digital state;

until the difference of all number pairs of said first and second sets of numbers are either added to or subtracted from the running sum of absolute values of the differences.

The examiner relies on the following prior art references:

Taniguchi 5,373,459 December 13, 1994
(filed April 17, 1992)

Hill, Fredrick J., and Peterson, Gerald R., Digital Systems: Hardware Organization and Design 596-99(2d ed., John Wiley & Sons 1978)(hereinafter "Hill").

Taniguchi, figure 6, discloses a circuit whose function "is to output the absolute value of the difference between the inputted two data" (col. 14, lines 26-27). The value of (X-Y) is formed in circuit 602 along with an overflow signal 609. The value of {X-(Y+1)} is formed in circuit 603 and the inverse {&&&&&&&&} is formed in circuit 604, where {&&&&&&&&} = -(X-Y) = the two's complement of (X-Y) (col. 12, equations 14 and 15). If the overflow is 0, the result of the subtraction (X-Y) is positive and the selection circuit 605 outputs the value of (X-Y), whereas if the overflow is 1, the result of the subtraction (X-Y) is negative and the selection circuit 605 outputs {&&&&&&&&} = -(X-Y) (col. 12, lines 51-57).

Hill describes multiplication with carry-save addition.

Claims 1, 3, and 4 stand rejected under 35 U.S.C. § 103 as being unpatentable over Taniguchi.

Claims 5-12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Taniguchi and Hill.

We refer to the second Office action entered February 21, 1995 (Paper No. 5), the Final Rejection (Paper No. 8) (pages referred to as "FR__"), and the Examiner's Answer (Paper No. 14) (pages referred to as "EA__") for a statement of the Examiner's position and to the Appeal Brief (Paper No. 13) (pages referred to as "Br__") and the Reply Brief (Paper No. 15) (pages referred to as "RBr__") for a statement of Appellants' arguments thereagainst.

OPINION

Group I - Claims 1, 3, and 4

The Examiner finds that Taniguchi discloses the claimed invention except (Paper No. 5, page 4):

> Taniguchi does not disclose keeping a running sum of the output absolute values. However, it was old and notoriously well known in the art at the time of the invention that a running sum was an appropriate method of summing multiple values, and therefore, this modification would have been obvious to one of ordinary skill in the art at the time of the invention.

Appellants argue "Taniguchi fails to teach the formation of the claimed 'sum of the absolute value of the difference'" (Br7). The Examiner recognized this difference and addressed it. Appellants do not address the Examiner's finding or conclusion.

It is proper for an examiner to make a finding of "well known" prior art if the knowledge is of such notorious character that Official Notice can be taken. Manual of Patent Examining Procedure § 706.02(a) (5th ed., Rev. 14, Nov. 1992), now in § 2144.03 (6th ed., Rev. 3, July 1997). It takes very little on the part of an applicant to traverse such a finding. Applicant need merely assert for the record that the examiner is wrong or that the applicant is not aware that the fact is well known, i.e., either deny or state that he is without knowledge or information sufficient to form a belief as to the truth of the finding, similar to responding in an answer to the claims of a complaint under Fed. R. Civ. P. 8(b). That way the Patent and Trademark Office does not spend time proving matters which are, in fact, known by the applicant. The examiner should then produce evidence to support the finding. Challenging the existence of well known prior art by

arguing that the fact is not supported by a reference, without stating that the examiner is wrong or that applicant is without knowledge of the prior art teaching does not constitute a proper traverse.

The Examiner's finding that running sums were well known in the prior art is not the kind of fact which lends itself to Official Notice. Although we agree that accumulation of sums was well known in the field of computer arithmetic, using Official Notice instead of supplying a reference is a difficult fact to review in any subsequent judicial review where the judges will not have the technical background of the examiner, the applicant, or the Board panel. Cf. In re Ahlert, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970)("Assertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art."); accord In re Pardo, 684 F.2d 912, 917, 214 USPQ 673, 677 (CCPA 1982). However, since the Examiner has continuously maintained his position and Appellants have not argued that the Examiner erred, we conclude that adding the absolute value

Z = #X-Y# in Taniguchi to a running sum of absolute values of the differences would have been obvious.

Appellants refer to the following language of claim 1:

> conditionally either 1) adding said difference to a running sum of the absolute values of the differences if said status bit is said first digital state, or 2) subtracting said difference from the running sum of absolute values of the differences if said status bit is said second digital state . . . .

Appellants argue that this "language of claim 1 requires that only one of the two possible operations of (1) adding the difference and of (2) subtracting the difference is performed" (Br5) and "specifically excludes the possibility that both the adding and subtracting operations are performed" (Br5). Appellants argue that "[f]ollowing the teachings of Taniguchi clearly results in computation of two results and the conditional discarding one of them" (Br6).

The Examiner responds that "[t]he claim language 'comprising' does not exclude the possibility that both operations are performed and either one of the outcomes is selected conditionally" (EA6). Appellants respond that "the 'either ... or' language excludes the possibility that the claim covers performing both the recited operations and selecting the indicated result" (RBr2).

Appellants' arguments are not supported by the claim language. As discussed above, we conclude that adding the absolute value Z = #X-Y# in Taniguchi to a running sum of absolute values of the differences would have been obvious because Appellants did not challenge the Examiner's rejection on this point. Thus, Taniguchi would conditionally either add (X-Y) to the running sum of absolute values of the differences at the output if (X-Y) was positive or would add -(X-Y) to the running sum of absolute values of the differences at the output if (X-Y) was negative (one of ordinary skill in the art of computer arithmetic would have recognized that adding -(X-Y) is the same as subtracting (X-Y)). Taniguchi does not both add the difference to the running sum and subtract the difference from the running sum and then discard one result as argued by Appellants. Taniguchi does compute both the difference and the two's complement of the difference and discards one, but this is not precluded by claim 1.

Appellants refer to the limitation in claim 1 that recites "forming a sum of the absolute value of the difference between each pair of numbers of respective first and second sets of numbers." Appellants argue that Taniguchi "teaches

only the formation of the absolute value of a single pair of numbers" (Br7) and "[t]he FINAL REJECTION fails to point out any portion of Taniguchi teaching or suggesting the formation of a sum of plural such absolute values" (Br7).

As discussed, the Examiner stated that "it was old and notoriously well known in the art at the time of the invention that a running sum was an appropriate method of summing multiple values, and therefore, this modification would have been obvious to one of ordinary skill in the art at the time of the invention" (Paper No. 5, page 4). This discussion of a running sum indicates that it is the Examiner's position that the circuit of Taniguchi is applied to a series of number pairs. As stated more clearly in the Examiner's Answer (EA3-4):

> Taniguchi's method is not limited to one particular set of inputs X and Y to produce one and only [one] output absolute value Z. One skilled in the art can [sic, could have] easily recognize[d] that more than one absolute value Z can be obtained from the selection circuit 605.

And (EA5):

> [T]he exemplary embodiments disclosed by Taniguchi are not limited to only one set of X and Y inputs for only one absolute value Z . . . . Therefore, it would have been an obvious modification for one of ordinary skill in the art to input a series of first and second multi-bit

> input signals as suggested by Taniguchi and obtain a series of absolute values.

We agree with the Examiner that it would have been obvious to one of ordinary skill in the art to form a series of absolute values of differences from a first and second series of numbers, one pair at a time. Claim 1 does not require that the differences and absolute values are formed in parallel by simultaneous operations as in claim 6; the operations can be performed serially. Moreover, claim 1 does not require that the "first and second sets of numbers" contain more than one number per set; it does not require plural number pairs.

Appellants argue that "Taniguchi fails to teach or suggest direct computation of the running sum by subtraction as recited in claim 1" (Br8) and "the Examiner has made no arguments regarding this point in either the Office action of February 21, 1995 or the FINAL REJECTION" (Br8). Appellants further argue that "[t]he Examiner has never stated any argument how the combination of Taniguchi and Hill et al make obvious the addition to the running sum by subtraction as recited in claim 1" (RBr4).

The Examiner points to column 14, lines 52-65, for the teaching of subtraction (Paper No. 5, page 4), which teaching Appellants fail to address.

Taniguchi, as modified in light of the Examiner's finding of well known prior art discussed previously would conditionally either add (X-Y) to the running sum of absolute values of the differences at the output if (X-Y) was positive or would add -(X-Y) to the running sum of absolute values of the differences at the output if (X-Y) was negative. One of ordinary skill in the art of computer arithmetic would have recognized that adding -(X-Y) is subtracting (X-Y).

For these reasons, we conclude that the Examiner has presented sufficient evidence and argument to establish a prima facie case of obviousness. The rejection of claims 1, 3, and 4 is sustained.

Group II - Claim 5

Claim 5 recites "storing any carry output" from the step of conditionally adding or subtracting the difference to a running sum of the absolute values of the differences, "adding said carry output to a running sum of carry outputs," and "adding said running sum of carry outputs to said running sum

of absolute values of said differences" after the addition or substraction. As explained in the specification, the running sum of carry outputs accounts for the overflow bits from the partial sums (specification, page 274). "As a consequence a register of fixed size may be used to store the running sum regardless of the number of differences formed." (Br9.)

The Examiner applies Hill. The Examiner's position is (Paper No. 5, page 5):

> Hill discloses that carry-save addition includes storing the carry from an addition stage and then iteratively adding and storing succeeding carries in the carry save register (p. 598; fig. 15.4). It would have been an obvious modification to one of ordinary skill in the art at the time of the invention to modify Taniguchi to use a carry-save adder as disclosed by Hill, because a carry-save adder is particularly well suited for a situation in which a series of numbers is to be added together; this would be the situation in Taniguchi if a series of absolute values from the selection circuit, 605, were to be summed.

Appellants argue that the teachings of Hill would not lead to the running sum of carry outputs claimed. "On the contrary, Hill et al teaches that the carries are added during the next following addition operation." (Br9.) We agree. There is no suggestion in the multiplication method of Hill "adding said carry output to a running sum of carry outputs" as claimed and the Examiner has failed to show where this is

found in Hill. The fact that Hill generally involves carries does not meet the specifics of the claim limitations.

In addition, although we conclude that formation of the running sum of absolute value of the differences in Taniguchi would have been obvious in light of Appellants' lack of argument on this point, we are not willing to modify this modification to include "adding said running sum of carry outputs to said running sum of absolute values of said differences" as proposed by the Examiner's rejection without a specific teaching.

Appellants argue that the teachings of Hill would result in an incorrect answer (Br9-10). The Examiner asserts that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the techniques of Hill in view of Taniguchi to arrive at the claimed invention" (EA8). We do not see how one of ordinary skill in the art would reasonably be led to arrive at the claimed subject matter from the multiplication technique of Hill even using hindsight.

For these reasons, the Examiner has failed to establish a prima facie case of obviousness. The rejection of claim 5 is reversed.

Group III - Claims 6 and 7
Group IV - Claim 8

Appellants argue (Br11) that the combination of Taniguchi and Hill fails to make obvious the following limitations of claim 6: (1) "simultaneously forming a predetermined plurality of differences between" (emphasis added) respective pairs of numbers; (2) "simultaneously for all of said predetermined plurality of differences conditionally either 1) adding . . . or 2) subtracting a particular one of said plurality of differences from said respective one of said plurality of running sums of absolute values of differences"; and (3) "thereafter adding said plurality of running sums of absolute values of differences to form the sum of the absolute value of the difference between each pair of numbers of respective first and second sets of numbers." Appellants argue that neither the Office action of February 21, 1995, nor the Final Rejection include any reference to this subject matter.

The closest we can find to any relevant reasoning by the Examiner is the following (EA5):

> [T]he exemplary embodiments disclosed by Taniguchi are not limited to only one set of X and Y inputs for only one absolute value Z, and Taniguchi further suggests the use of first and second multi-bit input signals (see column 14, line 43, and column [?][)]. Therefore, it would have been an obvious modification for one of ordinary skill in the art to input a series of first and second multi-bit input signals as suggested by Taniguchi and obtain a series of absolute values.

This does not particularly address the claim limitations. An operation on a multi-bit numbers does not suggest simultaneous operations on a plurality of separate numbers, adding or subtracting the plurality of differences to a plurality of running sums of absolute values of the differences, and then adding the partial sums together. Since Taniguchi does not disclose a running sum of the absolute values of the differences clearly some reasoning is needed to demonstrate the obviousness of a plurality of running sums and then adding the sums together. The Examiner has made no argument that it would have been obvious to have a plurality of circuits in parallel and then to sum the partial sums from each circuit, or any other argument that would address the claim limitations. Thus, the Examiner has failed to establish

a prima facie case of obviousness. The rejection of claim 6 and dependent claims 7 and 8 is reversed.

Group V - Claims 9-11
Group VI - Claim 12

Claim 9 contains limitations about storing the carry output similar to claim 5 except that it more specifically recites "storing any carry output . . . in corresponding locations of a set of more significant bits of said multiple flags register" and "storing any carry output . . . in corresponding locations of said set of least significant bits of said multiple flags register" before "adding said number of carry outputs to a running sum of carry outputs," whereas claim 5 only recites storing any carry output and adding the carry output to a running sum of carry outputs. Claim 9 also contains limitations similar to those addressed in connection with claim 6 except that it recites performing the plurality of differences operation twice and, thus, it recites a "first" and a "second" plurality of differences. Therefore, claim 9 is narrower than claim 5 in regard to the carry output limitations and is narrower than claim 6 in regard to the plurality of differences and the addition of the running sums than claim 6. For the reasons stated in connection with the

rejection of claims 5 and 6, the rejection of claim 9 and dependent claims 10-12 is reversed.

CONCLUSION

The rejection of claims 1, 3, and 4 is sustained.

The rejection of claims 5-12 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JERRY SMITH Administrative Patent Judge	)
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
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